**­­­­Fet­ch**   **T0** **: AR ← PC**

**T1 : IR ← M[AR] , PC ← PC + 1**

**Decode T2 : D0,……D7 ← Decode IR(4-6),**

**AR ← IR(0-3), I ← IR(7)**

**Indirect D’7IT3 : AR ← M[AR]**

**→**  **Memory – reference :**

**AND D0T4 : DR ← M[AR]   
 D0T5 : AC ← AC ^ DR , SC ← 0**

**ADD D1T4 : DR ← M[AR]   
 D1T5 : AC ← AC +DR , E ← COU1,  SC← 0**

**LDA D2T4 : AC ←M[AR]   
 D2T5 : AC ← DR, SC ← 0**

**STA D3T4 : M[AR] ← AC, SC ← 0**

**OR D4T4 : DR ← M[AR]   
 D4T5 : AC ← AC** || **DR ,  SC← 0**

**XOR D5T4 : DR ← M[AR]   
 D5T5 : AC ← AC +**  **DR , SC ← 0**

**→ Register – reference :**

**D7I’T3= r ( common to all register – reference instructions )**

**IR(i) = Bi ( i = 0 , 1 , 2 , 3 )**

**CLA rb3 : AC ← 0**

**CMA rB2 : AC ← AC**

**CIR rB1 : AC ← shr AC , AC(7) ←E , E ←AC(0)**

**CIL rB0 : AC ← shl AC , AC(0) ←E , E ←AC(15)**

**INC rB0B1 : AC ← AC + 1**

**HILT rB0B1B2 : S ← 0**

**→ Output / Input – reference :**

**D7IT3 = p ( Common to all input / output instruction )**

**IR(i) = Bi ( i = 0 , 1 )**

**INP pB3 : AC(0-7)** ← INPR

**OUT pB2 : OUTR** ←  **AC(0 – 7 )**